AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A pulse width modulation controlling circuit for a power supply comprising:

a processor means for generating a time-length signal comprising a first and second portion that indicate the pulse width;

a counting means for receiving said first portion of said time-length signal and counting in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said counting means outputting said coarse adjusted signal;

a delay means operatively connected to said counting means for receiving said coarse adjusted signal; and

a selection means coupled to said delay means for receiving said second portion of said time-length signal and for selecting a predetermined discrete delay period in said delay means, for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

2. (Original) The apparatus of claim 1, wherein said counting means is a digital counting means.

3. (Original) The apparatus of claim 2, wherein said digital counting means comprises a programmable logic device.

4. (Original) The apparatus of claim 3, wherein said counting means comprises an oscillator means operating at a predetermined frequency.

5. (Original) The apparatus of claim 4, wherein said oscillator means oscillates at approximately 125 MHz.

6. (Original) The apparatus of claim 1, wherein said delay means delays in increments of 0.25 nanoseconds.

7. (Original) The apparatus of claim 1, wherein said delay means is an analog delay means.

8. (Original) The apparatus of claim 1, wherein said delay means is a digital delay means.

9. (Original) The apparatus of claim 7, wherein said delay means comprises a plurality of inductors and capacitors connected in a series-parallel configuration.

10. (Original) The apparatus of claim 1, wherein said selection means is a digital selection means.

11. (Original) The apparatus of claim 9, wherein said selection means is a multiplexor.

12. (Original) The apparatus of claim 1, wherein said processor means operates at a first voltage, and said counting means, delay means, and selection means operates at a second voltage.

13. (Original) The apparatus of claim 12, wherein said apparatus further comprises a first and second transforming means, a power converter means, and a power conditioning means, wherein an output of said processing means is coupled to said first transforming means for transforming said output of said processing means at said first voltage to said second voltage, and an output of said second selection means is coupled to said power converting means, said second transformer means, and said power conditioning means.

14. (Original) The apparatus of claim 1, wherein said counting means, said delay means and said selection means are disposed in said processing means.

15. (Currently Amended) A method for controlling a switchmode power supply comprising:

generating a time-length signal that includes a first portion and a second portion that indicate a pulse duration of an output signal;

transmitting ~~a~~ the first portion of said time-length signal to a counting means, and ~~a~~ the second portion of said time-length signal to a selection means;

counting to a number based on said first portion of said time-length signal received by said counting means;

outputting a coarse adjusted signal from said counting means after counting to said predetermined number;

selecting a delay from a delay means based on said second portion of said time-length signal received by said selection means;

delaying said coarse adjusted signal a predetermined length of time based on said selected delay in said delay means; and

outputting ~~an~~ the output signal after said predetermined delay.

16. (Currently Amended) A pulse width modulation controlling circuit for a power supply comprising:

a processor means for generating a time-length signal comprising a first and second portion that indicate the pulse width;

a first selection means for receiving said first portion of said time-length signal, and for selecting one of a plurality of counting means, wherein said selected one of said plurality of counting means receives said first portion of said time-length signal and counts in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said selected one of said plurality of counting means outputting said coarse adjusted signal;

a delay means operatively connected to said counting means for receiving said coarse adjusted signal; and

a second selection means coupled to said delay means for receiving said second portion of said time-length signal and for selecting a predetermined discrete delay period in said delay means, for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

17. (Original) The apparatus of claim 16, wherein each one of said plurality of counting means counts at a unique, predetermined rate.

18. (Original) The apparatus of claim 16, wherein said plurality of counting means are digital counting means.

19. (Original) The apparatus of claim 16, wherein said each one of said plurality of counting means comprises a programmable logic device.

20. (Original) The apparatus of claim 16, wherein said counting means comprises an oscillator means operating at a predetermined frequency.

21. (Original) The apparatus of claim 16, wherein said delay means is an analog delay means.

22. (Original) The apparatus of claim 16, wherein said delay means is a digital delay means.

23. (Original) The apparatus of claim 21, wherein said delay means comprises a plurality of inductor and capacitors connected in a series-parallel configuration.

24. (Original) The apparatus of claim 16, wherein said first selection means is a digital selection means.

25. (Original) The apparatus of claim 24, wherein said first selection means is a multiplexor.

26. (Original) The apparatus of claim 16, wherein said second selection means is a digital selection means.

27. (Original) The apparatus of claim 26, wherein said second selection means is a multiplexor.

28. (Previously Presented) The apparatus of claim 16, wherein said processor means operates at a first voltage, and said first selection means, said plurality of counting means, delay means, and second selection means operates at a second voltage.

29. (Original) The apparatus of claim 28, wherein said apparatus further comprises a first and second transforming means, a power converter means, and a power conditioning means, wherein an output of said processing means is coupled to said first transforming means for transforming said output of said processing means at said first voltage to said second voltage, and an output of said second selection means is coupled to said power converting means, said second transformer means, and said power conditioning means.

30. (Original) The apparatus of claim 16, wherein said counting means, said delay means and said selection means are disposed in said processing means.

31. (Currently Amended) A pulse width modulation controlling circuit for a power supply comprising:

a processor for generating a time-length signal comprising a first portion and second portion that indicate the pulse width;

a counting circuit for receiving said first portion of said time-length signal and counting in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said counting circuit outputting said coarse adjusted signal;

a delay selection circuit for receiving said second portion of said time-length signal;

a plurality of delay circuits operatively connected to said plurality of counting means for receiving said coarse adjusted signal; and

a plurality of second selector circuits wherein said delay selection circuit selects one of said plurality of second selector circuits, and wherein a second selector circuit is coupled to each one of said plurality of delay circuits, said selected one of said plurality of second selector circuits for selecting a predetermined discrete delay period in one of said plurality of delay circuits, for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

32. (Previously Presented) The apparatus of claim 31, wherein said counting circuit is a digital circuit.

33. (Previously Presented) The apparatus of claim 32, wherein said digital counting circuit comprises a programmable logic device.

34. (Previously Presented) The apparatus of claim 33, wherein said counting circuit comprises an oscillator operating at a predetermined frequency.

35. (Previously Presented) The apparatus of claim 34, wherein said oscillator oscillates at approximately 125 MHz.

36. (Previously Presented) The apparatus of claim 31, wherein said delay circuit delays in increments of 0.25 nanoseconds.

37. (Previously Presented) The apparatus of claim 31, wherein said delay selection circuit is a digital circuit.

38. (Previously Presented) The apparatus of claim 37, wherein said delay selection circuit is a multiplexor.

39. (Previously Presented) The apparatus of claim 31, wherein said plurality of second selector circuits are digital circuits.

40. (Previously Presented) The apparatus of claim 39, wherein said plurality of second selector circuits are multiplexors.

41. (Previously Presented) The apparatus of claim 31, wherein each one of said plurality of delay circuits delays said coarse adjusted signal in unique, predetermined increments.

42. (Previously Presented) The apparatus of claim 31, wherein each one of said plurality of delay circuits is an analog circuit.

43. (Previously Presented) The apparatus of claim 42, wherein each one of said plurality of delay circuits comprises a plurality of inductor and capacitors connected in a series-parallel configuration.

44. (Previously Presented) The apparatus of claim 31, wherein each one of said plurality of delay circuits is a digital circuit.

45. (Previously Presented) The apparatus of claim 31, wherein said processor circuit operates at a first voltage, and said counting circuit, delay selection circuit, plurality of delay circuits, plurality of second and said selector circuits, operates at a second voltage.

46. (Previously Presented) The apparatus of claim 45, wherein said apparatus further comprises a first and second transforming circuit, a power converter circuit, and a power conditioning circuit, wherein an output of said processing circuit is coupled to said first transforming circuit for transforming said output of said processing circuit at said first voltage to said second voltage, and an output of each one of said plurality of second selector circuits, said selection circuit is coupled to power converting circuit, said second transformer circuit, and said power conditioning circuit.

47. (Previously Presented) The apparatus of claim 31, wherein said counting circuit, said delay circuit and said selection circuit are disposed in said processor.

48. (Currently Amended) A pulse width modulation controlling circuit for a power supply comprising:

a processor for generating a time-length signal comprising a first and second portion that indicate the pulse width;

a first selector for receiving said first portion of said time-length signal, and for selecting one of a plurality of counters, wherein said selected one of said plurality of counters receives said first portion of said time-length signal and counts in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said selected one of said plurality of counting means outputting said coarse adjusted signal;

a delay selector for receiving said second portion of said time-length signal;

a plurality of delay elements operatively connected to said plurality of counters for receiving said coarse adjusted signal; and

a plurality of second selectors, wherein said delay selector selects one of said plurality of second selectors, and wherein a second selector is coupled to each one of said plurality of delay elements, said selected one of said plurality of second selectors for selecting a predetermined discrete delay period in one of said plurality of delay elements, for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

49. (Previously Presented) The apparatus of claim 48, wherein each one of said plurality of counting counters counts at a unique, predetermined rate.

50. (Previously Presented) The apparatus of claim 48, wherein said plurality of counters are digital counters.

51. (Previously Presented) The apparatus of claim 48, wherein said first selector is a digital selector.

52. (Previously Presented) The apparatus of claim 48, wherein said first selector is a multiplexor.

53. (Previously Presented) The apparatus of claim 48, wherein said delay element is a digital delay element.

54. (Previously Presented) The apparatus of claim 53, wherein said delay selectors is a multiplexor.

55. (Previously Presented) The apparatus of claim 48, wherein said plurality of second selectors are digital selectors.

56. (Previously Presented) The apparatus of claim 55, wherein said plurality of second selectors are multiplexors.

57. (Previously Presented) The apparatus of claim 48, wherein each one of said plurality of delay elements delays said coarse adjusted signal in unique, predetermined increments.

58. (Previously Presented) The apparatus of claim 48, wherein each one of said plurality of delay elements is an analog element.

59. (Previously Presented) The apparatus of claim 58, wherein each one of said plurality of delay elements comprises a plurality of inductor and capacitors connected in a series-parallel configuration.

60. (Previously Presented) The apparatus of claim 48, wherein each one of said plurality of delay elements is a digital delay element.

61. (Previously Presented) The apparatus of claim 48, wherein said processor operates at a first voltage, and said first selector, plurality of counters, delay selectors, plurality of delay elements and said plurality of second selectors operates at a second voltage.

62. (Previously Presented) The apparatus of claim 61, wherein said apparatus further comprises a first and second transform circuit, a power converter, and a power conditioner, wherein an output of said processor is coupled to said first transform circuit for transforming said output of said processor at said first voltage to said second voltage, and an output of each one of said plurality of second selectors is coupled to said power converter, said second transform circuit, and said power conditioner.

63. (Previously Presented) The apparatus of claim 48, wherein said counter, said delay element and said selector are disposed in said processor.

64. (Currently Amended) A method for controlling a switchmode power supply in a plasma chamber comprising:

generating a time-length signal that includes a first portion and a second portion that indicate a pulse duration of an output signal;

transmitting ~~a~~ the first portion of said time-length signal to a counting circuit, and ~~a~~ the second portion of said time-length signal to a selection circuit;

counting to a number based on said first portion of said time-length signal received by said counting circuit;

outputting a coarse adjusted signal from said counting circuit after counting to said predetermined number;

selecting a delay from a delay circuit based on said second portion of said time-length signal received by said selection circuit;

delaying said coarse adjusted signal a predetermined length of time based on said selected delay in said delay circuit; and

outputting ~~an~~ the output signal to said power supply in said plasma chamber after said predetermined delay.

65. (Previously Presented) The method of claim 64, wherein said counting circuit is a digital circuit.

66. (Previously Presented) The method of claim 65, wherein said digital counting circuit comprises a programmable logic device.

67. (Previously Presented) The method of claim 66, wherein said counting circuit comprises an oscillator means operating at a predetermined frequency.

68. (Previously Presented) The method of claim 67, wherein said oscillator oscillates at approximately 125 MHz.

69. (Previously Presented) The method of claim 64, wherein said delay circuit delays in increments of 0.25 nanoseconds.

70. (Previously Presented) The method of claim 64, wherein said delay circuit is an analog circuit.

71. (Previously Presented) The method of claim 64, wherein said delay circuit is a digital circuit.

72. (Previously Presented) The method of claim 70, wherein said delay circuit comprises a plurality of inductors and capacitors connected in a series-parallel configuration.

73. (Previously Presented) The method of claim 64, wherein said selection circuit is a digital selection circuit.

74. (Previously Presented) The method of claim 64, wherein said selection circuit is a multiplexor.

75. (Previously Presented) The method of claim 64, wherein said processor operates at a first voltage, and said counting circuit, delay circuit, and selection circuit operates at a second voltage.

76. (Previously Presented) The method of claim 75, wherein said apparatus further comprises a first and second transform circuit, a power converter, and a power conditioner, wherein an output of said processor is coupled to said first transform circuit for transforming said output of said processor at said first voltage to said second voltage, and an output of said second selection circuit is coupled to said power converter, said second transformer means is coupled to said power converting means, said second transform circuit, and said power conditioner.

77. (Previously Presented) The method of claim 64, wherein said counting circuit, said delay circuit and said selection circuit is disposed in said processor.

78. (Previously Presented) The method of claim 64, wherein the step of generating a time-length signal further comprises generating said time-length signal in a processor.

79. (Previously Presented) The method of claim 64, wherein said counting circuit is a digital circuit.